Silicon NPN Power Transistors 2SC3272

DESCRIPTION

·With TO-126 package
·High breakdown voltage

APPLICATIONS

·For power amplification

PINNING□see Fig.2□

PIN	DESCRIPTION
1	Emitter
2	Collector
3	Base

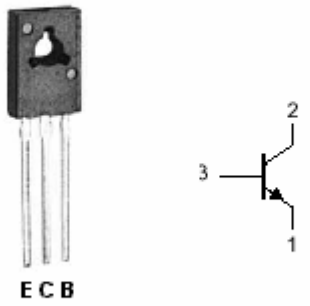

Fig.1 simplified outline (TO-126) and symbol

Absolute maximum ratings (Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	300	V
V_{CEO}	Collector-emitter voltage	Open base	300	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		0.1	A
I_{CM}	Collector current-peak		0.2	A
P_C	Collector power dissipation	T_C=25□	10	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CEsat}	Collector-emitter saturation voltage	I_C=50mA ;I_B=5m A			2.0	V
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C=10μA;I_E=0	300			V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=1mA; I_B=0	300			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=10μA; I_C=0	5			V
h_{FE}	DC current gain	I_C=10mA ; V_{CE}=10V	39		180	
I_{CBO}	Collector cut-off current	V_{CB}=200V; I_E=0			0.5	μA
I_{EBO}	Emitter cut-off current	V_{EB}=4V; I_C=0			0.5	μA
C_{OB}	Output capacitance	I_E=0; V_{CB}=30V;f=1MHz		3		pF
f_T	Transition frequency	I_C=10mA ; V_{CB}=30V	50			MHz

PACKAGE OUTLINE

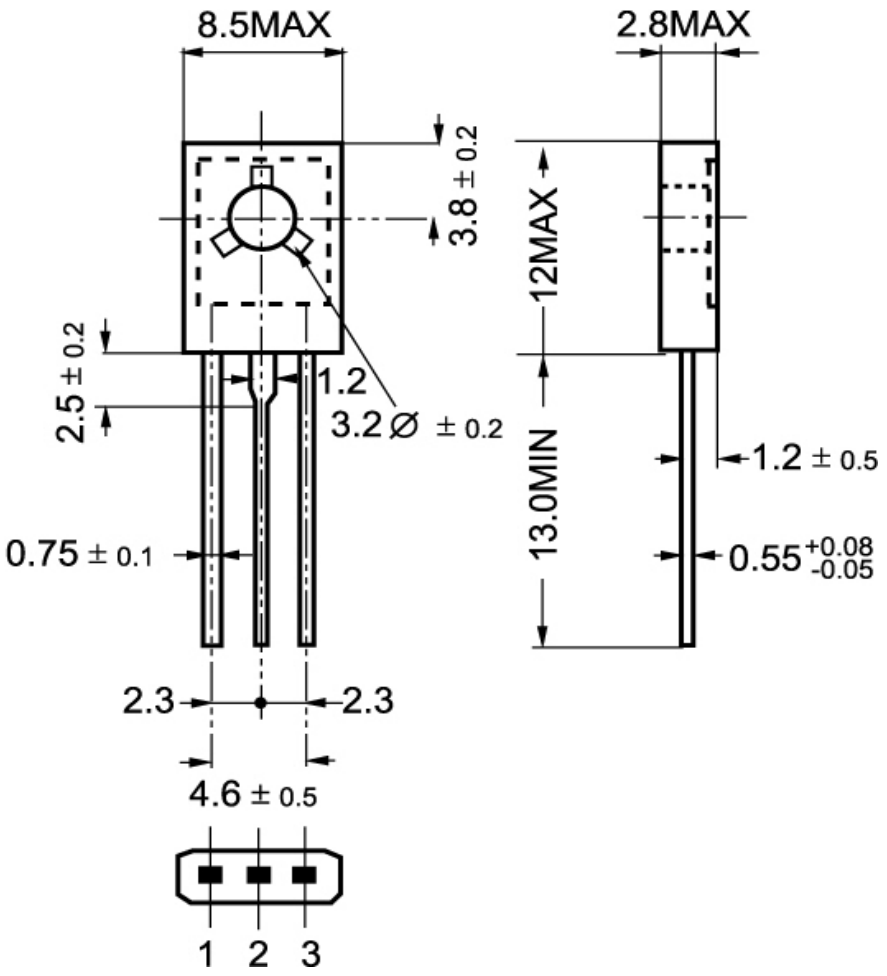

Fig.2 outline dimensions